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EXAMINER	
CAPUTO, LISA M	
ART UNIT	**PAPER NUMBER**
2876	

DATE MAILED: 04/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/920,752	MATSUMOTO, KEN	
	Examiner	Art Unit	
	Lisa M Caputo	2876	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Amendment

1. Receipt is acknowledged of the amendment filed 6 January 2004.

Double Patenting

2. Claim 32 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 30. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 21-29 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Roehrman et al. (U.S. Patent No. 4,010,355, from hereinafter "Roehrman").

Roehrman teaches a semiconductor wafer having machine readable indices and a method of reading the wafer. Regarding claim 21, Roehrman teaches an apparatus which reads a code (rows 18 and 20) formed on a substrate (12) which comprises a transfer unit with a holding member to hold and transfer the substrate (the wafer 12 is propelled along a suitable conveying means to a stop means at a read station), and a reading unit which optically reads a code formed on the substrate, at least a portion of

which is arranged on the transfer unit (the wafer is stopped at a read station where it is scanned with the read head 30 and released from the read station to continue its travel, hence the stop means is holding the wafer and it is also arranged on the transfer unit along with the reading means).

Roehrman discloses that turning now to the drawings, more particularly to FIG. 1, there is shown a plan view of the bottom surface 10 of a semiconductor wafer 12 having identifying indices 14 thereon in accordance with the invention. The semiconductor wafer 12 has a flat edge 16, provided in accordance with standard practice in the semiconductor device and integrated circuit manufacturing industry for orientation of the semiconductor wafer 12. The identifying indices are placed on the bottom surface 10 of the wafer 12 in a first row 18 and a second row 20 (as recited in claim 28 of the instant application). The first row 18 contains the actual identifying binary number for the wafer 12. The second row 20 contains the complement of the binary identification number in the first row 18, for error checking purposes. A sufficient explanation of the binary bar code (the code is a bar code as recited in claim 27 of the instant application) shown in FIG. 1 is contained in this application to allow understanding of the invention. For further details on the bar code employed, reference is made to a copending, commonly assigned application Ser. No. 448,171 filed Mar. 4, 1974 by Earlan Burk, entitled, "Bar Code Sequential Document Number Encoding With Error Checking," the disclosure of which is hereby incorporated by reference herein. In practice, a 28 position field is used for the identifying indices, although a lesser number has been shown in the drawing for purposes of clarity. The first position 22 and last position 24 of the field are used to mark

the start and the end of the data stream representing the identifying number on the wafer, and always contain a bar, which indicates a binary 1. The absence of a bar at a field position in the code represents a binary 0. The second position 26 of the 28 position field is a parity bit. If a bar is located in any bit position in row 18, no bar should appear at the corresponding position in line 20, as the sensed information would otherwise be cancelled out by the differential amplifier. The remaining 25 positions of the 28 position field contain the wafer identification number. This number of positions is chosen to be odd to insure that parity bit 26 is not 1 or 0 simultaneously in both rows. The bar code may be placed on the bottom surface 10 of the wafer 12 by any known method, such as a photoresist and etching step, or the like. In practice, it is preferred to use a laser scribing method, comparable to that employed for laser scribing for separation of the wafer 12 into individual semiconductor devices or integrated circuits. The wafer surface 10 may or may not contain an oxide over the scribed identifying indices. In practice, the bars 28 constituting the identifying code are 60 thousandths of an inch long, and spaced about 25 to 30 thousandths of an inch apart in the rows 18 and 20. The two rows are separated by 20 thousandths of an inch, and the row 20 is positioned 60 thousandths of an inch from flat edge 16 of the semiconductor wafer 12.

FIG. 2 represents a plan view of a preferred fiber-optic reading head 30 for use in the invention. The reading head 30 consists of a block 32 having a row 34 of light transmitting optical fibers 36 and a row 38 of light receiving optical fibers 40. In this embodiment, some optical fiber bundles 36 in row 34 are used to direct light to row 18 of the bar code and some other optical fiber bundles 36 are used to direct light at row 20

of the bar code. For example, the upper two bundles of row 34 can be used for row 18 of the bar code, and its bottom two can be used for row 20. The corresponding optical fiber bundles 40 in row 38 are used to detect light reflected from the corresponding row 18 or 20 of the bar code (as recited in claim 22 of the instant application). Since a position in one row of the bar code which contains a binary 1 will always be opposite a position in the other row containing a binary 0, i.e., the absence of a bar 28, the optical fibers for the row not containing a bar provides a background signal for subtraction from the data signal. This means that the optical fiber bundles serving to provide the reference signal change depending on which row 18 or 20 contain a binary 1. The embodiment shown depends on reflected light from the surface 10 of semiconductor wafer 12. Alternatively, if light in the infra-red wave length which may be transmitted through the silicon wafer 12 is employed, the light transmitting fiber optic 36 would be placed on one side of the wafer 12, and the light receiving fibers 40 would be placed on the other side of the wafer (reading unit includes a code detecting portion and a code illumination portion as recited in claims 23-24 of the instant application). When using reflected light in the invention, essentially any wavelength can be used that is reflected by the wafer surface 10. Ordinary incandescent light is suitable. However, it is not necessary that a visible light wavelength be used.

In operation, the read head 30 is scanned along the bar code row 18 and 20, such as by means of a pneumatic cylinder and piston, or solenoid. With automated wafer handling, the semiconductor wafer 12 is propelled along a suitable conveying means, such as a conventional semiconductor wafer air slide to a reading station. A

suitable stop means interrupts the wafer travel at the read station, the wafer is oriented by means of the flat edge 16, e.g., by rotating it with rollers until the flat 16 has reached the desired position (as recited in claim 25 of the instant application), the wafer is scanned with the read head 30, then the wafer is released from the read station to continue its travel along the air slide (read unit is formed on transfer unit as recited in claim 26 of the instant application) (see Figures 1-2, col 2 line 27 to col 3 line 63).

Regarding claims 29 and 31, Roehrman teaches, in addition to the above limitations outlined, that there is a processing unit and method in the form of circuitry for processing the output of the read circuit 41 for input to a computer. Roehrman discloses that FIG. 3 shows a schematic of a simple read circuit 41 that can be used in this invention. The read circuit 41 has first and second photo transistors 42 and 44 which are positioned so that the light transmitting optical fiber bundles for each row 18 and 20 of the bar code 14 impinge on one of the photo transistors 42 or 44. Photo transistor 42 is connected to one input of differential amplifier 46 by means of line 48. Photo transistor 44 is connected to the outer input of differential amplifier 46 by line 50. Photo transistors 42 and 44 are also connected to ground through resistors 52 and 54 by means of line 56 and 58 respectively. Output line 60 from differential amplifier 46 is connected to input line 48 of the differential amplifier by means of line 62 and resistor 64 in a conventional manner. Resistor 66 of differential amplifier input line 48 provides a matching impedance to resistor 64. As discussed previously, for each position in the field of the data code 14, one of the photo sensors 42 will provide a background signal for subtraction from the data signal supplied by the other photo sensor. Differential

amplifier 46 subtracts the background signal from the data signal, and the polarity of the resulting output pulse on output line 60 indicates which of the rows 18 or 20 of the identifying code 14 contains a binary 1 at the field position being sensed. This subtraction eliminates the DC portion of the background signal. In addition to a DC component, the background signal will normally contain peaks caused by surface irregularities on the bottom surface 10 of the semiconductor wafer 12, scratches and the like. Integrating circuit 63 is provided to convert these peaks to a DC signal level for subtraction by differential amplifier 46. Output line 60 from differential amplifier 46 is connected to one input of integrating circuit 63 by means of line 64 and resistor 66. The output of integrating circuit 63 is connected to photo sensor 44 by means of line 68. Terminal 70, connected to the other photo sensor 42, provides an operating voltage for the read circuit 41. The operation of integrating circuit 63 is conventional and will therefore not be further explained.

FIG. 4 shows in block diagram form additional circuitry for processing the output of read circuit 41 for input to a computer. Output 71 of read circuit 41 is connected to logic circuit 72. Output 74 of logic circuit 72 is connected to shift register 76. Data output line 60 of read circuit 41 is connected to threshold circuit 78. Threshold circuit 78 is connected to shift register 76 by line 80. Shift register 76 contains as many data positions as the field of identifying code 14 in FIG. 1, i.e., 28. The first and 28th data positions 82 and 84, respectively, are connected to gate 86 by line 88 and 90 respectively. Output 92 of gate 86 forms one input of gate 94. Output 96 of shift register 76 forms the other input to gate 94. Output 98 of gate 94 is connected to a computer

input. In operation of the circuitry of FIG. 4, the data from read circuit 41 is fed on line 60 to threshold circuit 78 for deletion of any remaining noise pulses in the data stream below the predetermined threshold, set to assure that only data pulses remain in the data stream. The data is supplied to shift register 76 by line 80. Logic circuit 72 is provided to remove the signals from positions 1 and 28 of the identifying code field, which are provided as end markers. For this purpose, the appropriate signals are provided on line 71 to logic circuit 72 to produce the required output pulses on line 74. A binary 1 must appear in both data positions 1 and 28 of the identifying code in order for the identifying data to be supplied to the computer on line 98. For this reason, the corresponding storage positions 82 and 84 of shift register 76 are connected to gate 86 and a binary 1 must appear on both line 88 and 90 to produce an enabling pulse for gate 94 on line 92, thus supplying the identifying data on line 96 through gate 94 to output line 98 (see Figures 3-4, col 3 line 64 to col 5 line 6).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 30 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roehrman in view of Goerigk (U.S. Patent No. 6,303,398). The teaching of Roehrman has been discussed above.

Regarding claims 30 and 32, Roehrman fails to disclose an exposure unit which performs an exposure process using the substrate based on the code read by the reading unit.

Goerigk teaches a method and system of managing wafers in a semiconductor device production facility. Goerigk discloses that in present semiconductor fabrication facilities, computer-aided manufacturing systems (CAM systems) control the fabrication process and provide information regarding operating conditions during these processes. Generally, the wafers undergo a specific treatment or process flow, i.e., the entirety of procedural steps necessary for forming a specific semiconductor device such as applying photoresist, irradiating the wafer with exposure light, developing the resist and etching the wafer, etc., to produce the desired device on the wafer. The wafers are generally stored in a single wafer cassette and are routed through the corresponding process stations to perform the desired process steps. One or more wafers to be subjected to a specific treatment form a specific lot of wafers. When the specific treatment is completed, a control unit, which may be implemented in a CAM system, instructs an operator or an automated transport system to transport the corresponding wafer cassette containing said lot of wafers, or at least a part of said wafer lot, to a new starting point for another process sequence or operation (see col 1, lines 45-65).

Further, the system shown in FIG. 1 will be described in its operational status with reference to FIGS. 1-4. The wafer sorter 5 is supplied with semiconductor wafers 11, each having a wafer identification mark 10 near a defined position. For example, the identification mark 10 may be placed near a notch or a flat 12 of the wafer 11 as is

shown in FIG. 2. In one embodiment, the wafer identification mark 10 consists of a 13 digit number which may contain a variety of information, such as the serial number of the wafer, type of dopant of the wafer, etc. The identification mark 10 may contain any desired information, and it may take any form that is readable by a machine or computer, e.g., a bar code, character strings, etc. (see Figures 1-4, col 4, lines 30-43). Hence, Goerigk teaches a system wherein a barcode contains information about different processes for a semiconductor wafer.

In view of the teaching of Goerigk, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ a system wherein the exposure process can be controlled by information read in a code because it is efficient to be able to control a wafer by accessing data on the code and having the process done automatically (i.e. more cost and time effective because the process is more quickly).

Response to Arguments

5. Applicant's arguments filed 6 January 2004 have been fully considered but they are not persuasive.

6. Applicant's arguments with respect to claims 30 and 32 have been considered but are moot in view of the new ground(s) of rejection.

7. In response to applicant's arguments that Roerhman does not provide a teaching or suggestion that the stop means is part of a reading unit or, it follows, that at least a portion of the reading unit is located on the transfer unit as recited in independent claims 21, 29, and 31, examiner respectfully disagrees. As taught above, Roehrman

specifically discloses that "the semiconductor wafer 12 is propelled along a suitable conveying means, such as a conventional semiconductor wafer air slide to a reading station" (see col 3, lines 50-56). This plainly teaches that the reading station is indeed located on the transfer unit. In addition, in order to be read, the wafer must be stopped, hence, the stopping means, in conjunction with the reading means (read head 30), are both located on the transfer unit in order to have a comprehensive system. The rejection stands (see 35 U.S.C. 102 rejection above).

In addition, examiner has found prior art to overcome the limitations in claims 30 and 32, hence they are not allowable. Any inconvenience to the applicant is regretted.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ***Lisa M. Caputo*** whose telephone number is **(571) 272-2388**. The examiner can normally be reached between the hours of 8:30AM to 5:00PM Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee can be reached at **(571) 272-2398.** The fax phone number for this Group is (703) 872-9306.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [**lisa.caputo@uspto.gov**].

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

LMC
April 16, 2004

DIANE I. LEE
PRIMARY EXAMINER